

Digigital design lab

Exp 5: Bit Parity Generator Circuit





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**Bit Parity Generator Circuit**

**Objective:**

Understanding the construction and applications of bit parity generators.

**Introduction:**

A bit parity, generated by the bit parity generator, usually accompanies the data transmission process. The bit parity provides as a reference point and allows us to compare and check whether the transmission process and the data transmitted are correct or not.

There are two types of bit parity generators: The "Odd" bit parity generator will generate an "1" if the data contains an even number of "1"s. For example, the data "10111011" has six "1"s. When the bit parity is added to the end of this data, the number of "1"s in the data will Become an 'ODD" number, hence the name "Odd Parity Generator".

On the other hand, an "Even" bit parity generator will add an "1" to data with odd number of "1"s to make the total number of "1"s even. If the data already has an even number of "1"s no bit panty is generated. Output Y of the "Even" bit parity generator shown in Fig. 4-1 will be 0 if the inputs ABCDEFGH is equal to 10111011.

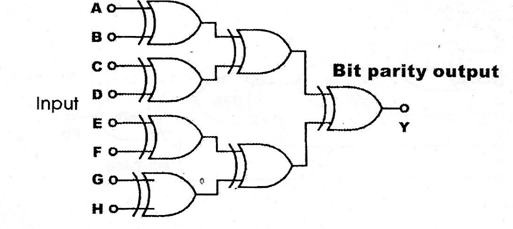


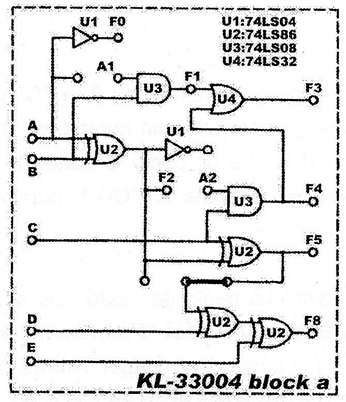
Fig. 5-1: Even bit parity generator circuit

REQUIRED EQUIPMENTS

* KL-31001 Digital Logic Lab
* Module KL-33003/4

PROCEDURES

1. **Bit Parity Generator Constructed with XOR Gates**
2. Insert connection clip according to Fig. 2-58 to construct the even bit parity generator circuit of Fig. 5-2.



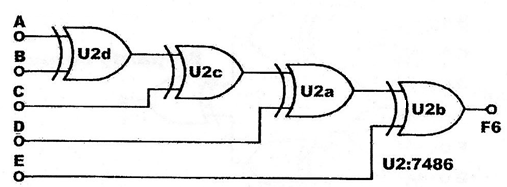


Fig. 5-2: Even bit parity generator circuit

1. Connect inputs A, B, C, D, E to DIP Switches 1.0-1.4 and output F6 to Logic Indicator L1. Follow the input sequences in Table 5-1 and record the outputs.

Table 5-1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| INPUT | | | | | OUTPUT |
| E | D | C | B | A | F6 |
| 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 | 0 |  |
| 0 | 0 | 0 | 1 | 1 |  |
| 0 | 0 | 1 | 0 | 0 |  |
| 0 | 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 1 | 0 |  |
| 1 | 1 | 0 | 0 | 0 |  |
| 1 | 1 | 0 | 1 | 0 |  |
| 1 | 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 | 1 |  |

1. **Bit Parity Generator 1C**
2. U7 on block d of module KL-33003 is a bit parity generator 1C. Connect inputs A1, B1. C1, D1, E1, F1, G1. H1 to DIP Switches 1.0-1,7 respectively. Connect outputs YO to L1; Y1 to L2, Follow the input sequences given in Table 5-2 and record the outputs.

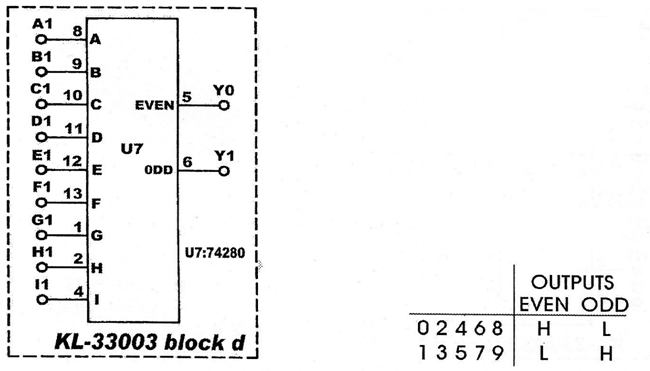


Fig. 5-3

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUT | | | | | | | | | OUTPUT |
| I | H | G | F | E | D | C | B | A | y0 y1  (even) (odd) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  |

**Table 4-2**

**Exercise**

**Construct a circuit that transmits 4-bit data with bit parity and see if the output are correct.**

**MULTIPLE CHOICE QUESTIONS**

1. The most convenient way to construct a bit parity generator is with :

1. XOR Gates.
2. AND Gates.
3. OR Gates.

2. If the data "11101" is transmitted with bit parity, what is its odd bit parity?

1. '1'
2. '0'
3. Neither

3. The purpose of generating bit parity is to:

a) For fun

b) For detection of errors

c) To increase data length

4. The correct way to detect errors during data transmission process is to:

a) Ask someone at the other end

b) Add bit parity

c) Observe outputs carefully